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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,091	07/22/2003	Takahiro Takemoto	NECA 20.522	8769

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EXAMINER	
PHAM, TAMMY T	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 06/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,091	TAKEMOTO, TAKAHIRO	
	Examiner	Art Unit	
	Tammy Pham	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,8-11,13-16 and 18-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,8-11,13-16 and 18-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Claims 1, 6, 11 and 16 have been amended. Claims 21-24 have been added. Claims 1, 3-6, 8-11, 13-16 and 18-24 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-6, 8-11, 13-16 and 18-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (US Patent No: 5,873,003) in view of the applicant's admitted prior art (AAPA).

As for claims 1, 11, Inoue teaches of active-matrix addressing LCD device and method (claim 11) comprising:

a panel including an active-matrix substrate, an opposite substrate, and a liquid crystal layer sandwiched by the active-matrix substrate and the opposite substrate; the active-matrix substrate having data lines, scanning lines that intersect with the data lines at intersections, pixels

arranged near the respective intersections, and TFTs arranged as switching elements for the respective pixels;

a source driver circuit for driving the data lines;

a gate driver circuit for driving the scanning lines; and

a controller circuit for controlling the source: driver and the gate driver;

wherein the source driver has a resetting means for resetting the data voltages outputted by the source driver circuit in a blanking period of each of the horizontal synchronizing periods of the set in column 19, lines 8-15; and

wherein the resetting means performs its resetting operation with reference to a latch signal supplied to the source driver circuit by the controller circuit. Please note that although Inoue has no mention of a latch, Inoue's teachings does meet the definition of the latch as defined by the applicant as "...temporarily latching the data in the source driver circuit..." as it is only inherent that the apparatus contains some kind of means to supply data to the source driver circuit and hence meets the claim limitations as currently stated.

Inoue fails to teach that a polarity of a data voltage applied to each of the pixels by way of a corresponding one of the data lines and a corresponding one of the TFTs is inverted in every set of two or more horizontal synchronizing periods by the controller circuit.

AAPA teaches that a polarity of a data voltage applied to each of the pixels by way of a corresponding one of the data lines and a corresponding one of the TFTs is inverted in every set of two or more horizontal synchronizing periods by the controller circuit in section [0014].

It would have been obvious to one with ordinary skill in the art at the time the invention was made to have the polarity of a data voltage applied to each of the pixels by way of a

corresponding one of the data lines and a corresponding one of the TFTs is inverted in every set of two or more horizontal synchronizing periods by the controller circuit as taught by AAPA with the active-matrix addressing device as taught by Inoue in order to prevent image quality degradation (AAPA: section [0011]).

As for claims 3, 13, the combination of Inoue and AAPA teaches that each of the data voltages alternately has a positive value or a negative value in the polarity inversion period; and wherein the resetting means is controlled in such a way that each of the data voltages will reach a middle point value between the positive value and the negative value after the resetting operation is completed in AAPA: section [0014]. The AAPA teaches that the polarity of the voltage is inverted with each period and Inoue teaches the reset voltage is applied during the blanking period so it naturally follows that the data voltages reach a middle point value between a negative and positive polarity between each blanking period.

As for claims 4-5, 9-10, 14-15, 19-20, the combination of Inoue and AAPA teaches that the polarity of the data voltages supplied by way of the data lines is alternately inverted in every set of the two horizontal synchronizing periods and in every vertical synchronizing period within every frame period, thereby driving the device by a 2-H dot inversion method (claim 4) and that

Within every frame period, thereby driving the device by a 2-H line inversion method (claim 5) in AAPA section [0014] and [0021].

As for claims 6, 16, Inoue teaches that the active-matrix addressing LCD device and method (claim 16) comprising:

a panel including an active-matrix substrate, an opposite substrate, and a liquid crystal layer sandwiched by the active-matrix substrate and the opposite substrate; the active-matrix substrate having data lines, gate lines that intersect with the data lines at intersections, pixels arranged near the respective intersections, and TFTs arranged as switching elements for the respective pixels;

a source driver circuit for driving the data lines;

a gate driver circuit for driving the scanning lines; and

a controller circuit for controlling the source driver and the gate driver;

wherein the source driver for the data voltages outputted by the source driver circuit in a blanking period of each of the horizontal synchronizing periods of the set

with reference to a latch signal which are supplied to the source driver circuit by the controller circuit.

Inoue fails to have any teachings to a polarity inverting means wherein a polarity of a data voltage applied to each of the pixels by way of a corresponding one of the data lines and a corresponding one of the, TFTs is inverted in every set of two or more horizontal synchronizing periods by the controller circuit; for inverting the polarity of the data voltages with reference to a latch signal and a polarity-inverting signal, which are supplied to the source driver circuit by the controller circuit.

AAPA teaches of a polarity inverting means wherein a polarity of a data voltage applied to each of the pixels by way of a corresponding one of the data lines and a corresponding one of

the, TFTs is inverted in every set of two or more horizontal synchronizing periods by the controller circuit; for inverting the polarity of the data voltages with reference to a latch signal and a polarity-inverting signal, which are supplied to the source driver circuit by the controller circuit in sections [0014].

It would have been obvious to one with ordinary skill in the art at the time the invention was made to have a polarity inverting means wherein a polarity of a data voltage applied to each of the pixels by way of a corresponding one of the data lines and a corresponding one of the, TFTs is inverted in every set of two or more horizontal synchronizing periods by the controller circuit; for inverting the polarity of the data voltages with reference to a latch signal and a polarity-inverting signal, which are supplied to the source driver circuit by the controller circuit with the active-matrix addressing device as taught by Inoue in order to prevent image quality degradation (AAPA: section [0011]).

As for claims 8, 18, the combination of Inoue and AAPA teaches that the polarity inverting means is controlled in such a way that each of the data voltages will reach a value of an opposite polarity after the polarity-inverting operation is completed in AAPA section [0014] and [0021].

As for claims 21-24, Inoue teaches of a method (claims 23,24) of driving an active-matrix addressing LCD device, the device comprising:

a panel including an active-matrix substrate, an opposite substrate, and a liquid crystal layer sandwiched by the active-matrix substrate and the opposite substrate; the active-matrix

substrate having data lines, scanning lines that intersect with the data lines at intersections, pixels arranged near the respective intersections, and TFTs arranged as switching elements for the respective pixels;

a source driver circuit for driving the data lines;

a gate driver circuit for driving the scanning lines; and

a controller circuit for controlling the source driver and the gate driver

wherein the source driver has a resetting means for resetting the data voltages outputted by the source driver in a blanking period of each of the horizontal synchronizing periods of the set (claims 21, 23) in column 19, lines 8-15;

Inoue fails to teach of a polarity of a data voltage applied to each of the pixels by way of a corresponding one of the data lines and a corresponding one of the TFTs is inverted in every set of two or more horizontal synchronizing periods by the controller circuit; a polarity inverting means for inverting the polarity of the data voltages outputted by the source driver circuit in a blanking period of each of the horizontal synchronizing periods of the set (claims 22, 24); and wherein the polarity of the data voltages supplied by way of the data lines is alternately inverted in every set of the two horizontal synchronizing periods and in every vertical synchronizing period within every frame period, thereby driving the device by a 2-H dot inversion method.

AAPA teaches that a polarity of a data voltage applied to each of the pixels by way of a corresponding one of the data lines and a corresponding one of the TFTs is inverted in every set of two or more horizontal synchronizing periods by the controller circuit; a polarity inverting means for inverting the polarity of the data voltages outputted by the source driver circuit in a blanking period of each of the horizontal synchronizing periods of the set (claims 22, 24); and

wherein the polarity of the data voltages supplied by way of the data lines is alternately inverted in every set of the two horizontal synchronizing periods and in every vertical synchronizing period within every frame period, thereby driving the device by a 2-H dot inversion method.

It would have been obvious to one with ordinary skill in the art at the time the invention was made to have a polarity of a data voltage applied to each of the pixels by way of a corresponding one of the data lines and a corresponding one of the TFTs is inverted in every set of two or more horizontal synchronizing periods by the controller circuit;a polarity inverting means for inverting the polarity of the data voltages outputted by the source driver circuit in a blanking period of each of the horizontal synchronizing periods of the set; and wherein the polarity of the data voltages supplied by way of the data lines is alternately inverted in every set of the two horizontal synchronizing periods and in every vertical synchronizing period within every frame period, thereby driving the device by a 2-H dot inversion method with the active-matrix addressing device as taught by Inoue in order to prevent image quality degradation (AAPA: section [0011]).

Response to Arguments

Applicant's arguments with respect to claims 1, 3-6, 8-11, 13-16 and 18-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tammy Pham whose telephone number is (571) 272-7773. The examiner can normally be reached on 8:00-5:30 (Mon-Fri).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tammy Pham
May 24, 2006

KENT CHANG
PRIMARY EXAMINER